Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

Claim 1 (previously presented): A method of implementing a digital communications link connecting a digital controller section of an xDSL modem, located on a system motherboard of a computing system, to a separate analog section of the xDSL modem adapted to be substantially free of electronic noise from other electronic components on the motherboard which could significantly affect the overall operation of such xDSL modem, said method comprising the steps of:

(a) providing a plurality of receive signal lines for communicating data from a remote xDSL modem;

(b) providing a plurality of transmit signal lines for communicating data to the remote xDSL modem;

(c) providing a bit clock signal line separate from said plurality of receive signal lines and said plurality of transmit signal lines for carrying a bit clock signal, which bit clock signal is generated by scaling a separate clock signal useable by the xDSL modem, such that said bit clock is variable to accommodate a plurality of different xDSL transmission protocols.

Claim 2 (previously presented): The method of claim 1, further including a step: providing a reset signal to reset the analog section of the xDSL modem.

Claim 3 (original): The method of claim 1, wherein at least four (4) signal lines are used for said receive signal lines, and at least (4) separate signal lines are used for said transmit signal lines.

Claim 4 (previously presented): The method of claim 1, further including a step of providing a word clock signal, which word clock signal has a cycle consisting of at least four (4) bit clock cycles, with the first cycle being a first value and the remaining cycles being a second value.

Claim 5 (original): The method of claim 1, wherein said receive and/or transmit signal lines can also be used for implementing an embedded operation channel within said receive and/or transmit signal lines, said embedded operation channel consisting of control signals embedded in both transmit and receive directions for use by the xDSL modem.

Claim 6 (original): The method of claim 4, wherein at least one (1) bit per word clock cycle is used to carry control signals.

Claim 7 (previously presented): The method of claim 5, wherein each control signal can have a first or a second length.

Claim 8 (original): The method of claim 5, wherein each control signal begins with a start bit, is followed by a length bit, then by a set of command bits, and then idle bits are sent between control signals.

Claim 9 (previously presented): The method of claim 1, further including a step: providing a multi-channel data frame during a plurality of consecutive bit clock periods based on said bit clock signal, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel

data frame, and through a second channel during a second time period of said multi-channel data frame, and further wherein said first and second time periods occur within said plurality of consecutive bit clock periods.

Claim 10 (previously presented): The method of claim 9, wherein the number of channels in the multi-channel data frame is programmable.

Claim 11 (previously presented): The method of claim 9, wherein said plurality of consecutive bit clock periods consists of at least four (4) bit clock cycles for each channel.

Claim 12 (previously presented): The method of claim 11, wherein the boundary of each multi-channel data frame is indicated by a separate word clock signal having a first predetermined value at the frame beginning and a second predetermined value in the rest of the frame.

Claim 13 (previously presented): The method of claim 1, wherein said receive and/or transmit signal lines can also be used to support a data interface between said digital controller and a hardware or DSP based xDSL modem.

Claim 14 (original): The method of claim 13, wherein the data interface is logically equivalent to a Utopia I and/or II interface and said hardware or DSP based xDSL modem also can perform an ATM transport convergence (TC) function.

Claim 15 (original): The method of 14, wherein an embedded operation channel (EOC) is used to control proper operations of the hardware or DSP based xDSL modem.

Claim 16 (previously presented): The method of claim 1, wherein said separate clock signal is based on a master clock external to the xDSL modem and operated at a frequency required by the digital communications link.

Claims 17-31 (canceled)

Claim 32 (previously presented): A method of implementing a digital communications link within a personal computer system, comprising the steps of:

(a) providing a plurality of receive signal lines, said receive signal lines being configurable such that data can be received by a digital controller from both an analog codec and an ATM interface;

(b) providing a plurality of transmit signal lines, said transmit signal lines being configurable such that data can be transmitted by a digital controller to both the analog codec and the ATM interface;

(c) providing a clock signal line, said clock signal line carrying a clock signal adapted for data transfers associated with both the analog codec and the ATM interface;

(d) providing a data transfer protocol such that data transfers over said digital communications link can include codec samples and/or ATM cell data;

wherein said clock signal further can be varied to accommodate a plurality of different data transfer protocols used in the digital communications link.

Claim 33 (original): The method of claim 32, wherein said ATM interface is logically equivalent to an ATM Utopia I and II interfaces.

Claim 34 (previously presented): The method of claim 32, wherein the digital controller is located on a system motherboard of the personal computer system, and said analog codec is located at a position which is substantially free of electronic noise from other electronic

components on said motherboard which could materially affect the operation of such analog codec.

Claim 35 (previously presented): The method of claim 32, wherein said digital communications link supports a plurality of data channels by time division multiplexing data transfers using a frame signal related to said clock signal.

Claim 36 (previously presented): The method of claim 32, wherein operational and/or control information for said analog codec can be embedded in data frames communicated through the plurality of receive and transmit signal lines.

Claims 37-60 (canceled)

Claim 61 (previously presented): In a motherboard for use in a personal computing system, and which system is configured to treat a high speed xDSL capable modem as a motherboard device, the improvement comprising:

(A) a digital controller associated with the high speed modem, said digital controller being located physically on the motherboard and including:

[i] circuitry for processing xDSL formatted data and control signals; and

(B) an analog front end circuit associated with the high speed modem, said analog front end circuit being electrically coupled but physically separated from said digital controller, said analog front end circuit including:

[i] line interface circuitry for coupling to a data channel carrying analog data signals corresponding to said xDSL formatted data and control signals; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and xDSL formatted data and control signals respectively; and

(C) a digital interface for coupling said digital controller and analog front end circuit, said digital interface including:

[i] a plurality of xDSL data receiving lines; and

[ii]a plurality of xDSL data transmitting lines; and

[iii] a clock signal adapted for an xDSL compatible link, said clock signal being generated by scaling a separate clock signal useable by the xDSL capable modem, such that said clock signal is variable to accommodate a plurality of different xDSL transmission protocols; and

wherein said digital interface supports an xDSL compatible data link between said digital controller and said analog front end circuit.

Claim 62 (original): The motherboard of claim 61, wherein said analog front end circuit is located on a riser card which is configured to be mounted substantially perpendicular to the motherboard.

Claim 63 (original): The motherboard of claim 61, wherein said digital controller is controlled in part in software by a host processor located on the motherboard.

Claim 64 (original): The motherboard of claim 61, further wherein said digital interface uses a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

Claim 65 (previously presented): The motherboard of claim 61, wherein said receive and/or transmit signal lines can also be used to support an Asynchronous Transfer Mode (ATM) interface.

Claim 66 (previously presented): The motherboard of claim 65, wherein said ATM interface is a Utopia I and/or II interface.

Claim 67 (previously presented): A method of transmitting data over an xDSL digital communications link between a digital controller portion of an xDSL modem and an analog codec portion of the xDSL modem, comprising the steps of:

(a) selecting an xDSL transmission protocol to be used in the xDSL digital communications link; and

(b) configuring a bit clock to accommodate transmission requirements of said selected xDSL transmission protocol, said bit clock being generated by scaling a separate clock signal useable by the xDSL modem; and

(c) communicating data between the digital controller portion of the xDSL modem and the analog codec portion of the xDSL modem across the xDSL digital communications link using said bit clock; and

(d) transmitting a frame of data across the xDSL digital communications link, said frame of data occupying a plurality of consecutive bit clocks;

wherein said bit clock is variable to accommodate a plurality of different xDSL transmission protocols, and wherein said frame of data is transmitted by dividing said frame of data over multiple communications lines.

Claim 68 (original): The method of claim 67, wherein said separate clock signal is a master clock signal used by the xDSL modem, and said bit clock is derived by dividing said master clock signal by a value specified for said xDSL transmission protocol.

Claim 69 (original): The method of claim 68, wherein said value specified for said xDSL transmission protocol is programmed and stored in a register of the analog codec portion of the xDSL modem.

Claim 70 (original): The method of claim 67, wherein the xDSL digital communications link is embodied as a bus located on a motherboard of a personal computer system.

Claim 71 (original): The method of claim 67, wherein said bit clock is used for both receive and transmit data.

Claim 72 (currently amended): The method of claim 67, further including a step: ~~(d)~~ (e) generating a word clock based on said bit clock for communicating data words between the digital controller portion of the xDSL modem and the analog codec portion of the xDSL modem across the xDSL digital communications link, said word clock having a period equal to a plurality of bit clock periods.

Claims 73-74 (cancelled)

Claim 75 (previously presented): The method of claim 67, wherein said frame of data is signalled by a word clock being held in an active state for more than one bit clock period.

Claim 76 (original): The method of claim 67, wherein said xDSL transmission protocols include Asymmetric Digital Subscriber Loop (ADSL) protocols.

Claim 77 (currently amended): The method of claim 67, wherein said data includes digital samples generated by an analog to digital converted forming part of the analog codec

portion of the xDSL modem, and said digital samples are processed by a host signal processing circuitry to support the xDSL modem.

Claim 78 (currently amended): The method of claim ~~67~~ 77, wherein said host signal processing circuitry includes a FFT circuit embedded in a digital controller as well as software executing on a host processor.

Claim 79 (original): The method of claim 67, wherein said data includes Asynchronous Transfer Mode (ATM) based data cells, and said ATM based data cells are processed by a hardware based signal processor to support the xDSL modem.

Claim 80 (cancelled)

Claim 81 (original): The method of claim 67, wherein step (c) is performed by the analog codec portion of the xDSL modem which is located on a separate board from the digital controller.

Claim 82 (original): The method of claim 67, wherein said bit clock can have a frequency exceeding 35 Mhz.

Claim 83 (previously presented): A digital communications link connecting a digital controller section of an xDSL modem located on a system motherboard of a computing system, to a separate analog section of the xDSL modem adapted to be substantially free of electronic noise from other electronic components on the motherboard which could significantly affect the overall operation of such xDSL modem, the digital communications link comprising:

(a) a plurality of receive signal lines for communicating data received by the analog section from a remote xDSL modem to the digital controller;

(b) a plurality of transmit signal lines communicating data received by the analog section from the digital controller to the remote xDSL modem;

(c) a bit clock signal line, separate from said plurality of receive signal lines and said plurality of transmit signal lines, for carrying a bit clock signal to clock transfers between the analog section and the digital controller;

wherein said bit clock signal has a variable frequency that can be set to accommodate a plurality of different xDSL transmission protocols.

Claim 84 (previously presented): The digital communications link of claim 83, wherein said bit clock can have a frequency exceeding 35 Mhz.

Claim 85 (cancelled)

Claim 86 (previously presented): The digital communications link of claim 83, wherein said bit clock signal is generated by the separate analog section of the xDSL modem on a modem riser card.

Claim 87 (cancelled)

Claim 88 (previously presented): The digital communications link of claim 83, wherein the digital controller section is incorporated within a motherboard for a computer system.

Claims 89-91 (cancelled)

Claim 92 (previously presented): A communications protocol for transmitting data over a digital communications link within a computer system between a digital controller and an analog coder/decoder (CODEC), the protocol comprising the steps of:

(a) generating a bit clock adapted for data transmission requirements of the digital communications link;

(b) generating a separate frame signal for indicating a boundary for a variable sized data frame transmitting the data between the digital controller and the analog CODEC;

(c) supporting a scaleable data rate in the digital communications link by adjusting a clock rate of said bit clock and/or a size of said variable sized data frame;

wherein said size of said variable sized data frame is adjusted by changing a number of active data channels used in the digital communications link.

Claim 93 (original): The communications protocol of claim 92 wherein said clock rate is varied in accordance with an xDSL transmission standard used in the digital communications link.

Claim 94 (cancelled)

Claim 95 (previously presented): The communications protocol of claim 92 wherein said number of active data channels can be varied in both a transmit and receive direction in the digital communications link.

Claim 96 (previously presented): The communications protocol of claim 92 wherein said number of active data channels is programmed by the digital controller.

Claim 97 (previously presented): The communications protocol of claim 92 wherein said number of active data channels is used to support a plurality of separate communication links with a plurality of respective separate analog codecs.

Claim 98 (original): The communications protocol of claim 92 wherein said frame signal is based on a word clock signal, said word clock signal being used for clocking a sample data word from an analog to digital (A/D) converter in the CODEC.

Claim 99 (original): An input/output (I/O) circuit for supporting a communications link over a computer bus used within a computer system between a digital controller and an analog coder/decoder (CODEC), the I/O circuit including:

a digital communications interface including:

1) a plurality of receive lines for receiving data; and

2) a plurality of transmit lines, separate from said plurality of receiving lines, for transmitting data;

wherein the data is transferred in parallel across said plurality of receive lines and said plurality of transmit lines in accordance with the bus protocol;

3) a bit clock signal line, separate from said plurality of receive signal lines and said plurality of transmit signal lines, for carrying a bit clock signal adapted for a transmission protocol supported by the bus protocol;

4) a frame clock signal line for carrying a frame clock signal adapted for clocking a variable sized data frame in accordance with the bus protocol, said variable sized data frame having a size based on a number of active channels in the plurality of separate data channels and/or a desired data rate;

wherein said plurality of receive lines, said plurality of transmit lines, said bit clock signal line and said frame clock signal line support the bus protocol as part of the communications bus within the personal computer system.

Claim 100 (currently amended): The I/O circuit of claim 99 wherein ~~said~~ a clock rate of said bit clock signal is varied in accordance with an xDSL transmission standard used in the digital communications link.

Claim 101 (original): The I/O circuit of claim 99 wherein said size of said variable sized data frame is adjusted by changing a number of active data channels used in the digital communications link.

Claim 102 (original): The I/O circuit of claim 101 wherein said number of active data channels can be varied in both a transmit and receive direction in the digital communications link.

Claim 103 (original): The I/O circuit of claim 101 wherein said number of active data channels is programmed by the digital controller.

Claim 104 (original): The I/O circuit of claim 101 wherein said number of active data channels is used to support a plurality of separate communication links with a plurality of respective separate analog CODECs.

Claim 105 (original): The I/O circuit of claim 99 wherein said frame signal is based on a word clock signal generated by the digital interface, said word clock signal being used for clocking a sample data word from an analog to digital (A/D) converter in the CODEC.

Claims 106-112 (canceled)

Claim 113 (previously presented): A method of communicating data over a data link connecting a first integrated circuit located on a first circuit board and a second integrated circuit located on a second circuit board, the method comprising the steps of:

(a) communicating first transmit data from the first integrated circuit to the second integrated circuit over the data link using a first transmission channel;

(b) communicating first receive data from the second integrated circuit to the first integrated circuit over the data link using a first receive channel, said first receive channel and said first transmission channel being separate;

(c) clocking data transmissions in said first transmission channel and/or said first receive channel over the data link using a scaleable clock signal;

(d) setting up a second transmission channel and a second receive channel over the data link between the first integrated circuit and a third integrated circuit to support second transmit data and second receive data respectively using said scaleable clock signal;

wherein said scaleable clock signal is adjusted for the data link between the first integrated circuit and the second integrated circuit so that the data link uses a scaleable clock rate to support a data transfer rate required for said first transmission channel and/or said first receive channel.

Claims 114-116 (cancelled)

Claim 117 (original): The method of claim 113 wherein said scaleable clock signal is a bit clock used in both said first transmit channel and said first receive channel.

Claim 118 (previously presented): The method of claim 113 wherein said data link is set up over a computer bus located on the first circuit board.

Claim 119 (cancelled)

Claim 120 (original): The method of claim 113 further including a step: time division multiplexing control information and data over said first transmission channel so as to provide control information from the first integrated circuit to said second integrated circuit as part of said data transmission, said control information including a power management signal including at least a wake-up signal and/or a power down signal.